

Application No.: 09/843,573  
Response to OA dated: 9/10/04  
Reply/Amendment dated: 3/10/05

In the Claims:

Please amend Claims 1 and 10, all as shown below. Applicant reserves the right to prosecute any originally presented or canceled claims in a continuing or future application.

1. (Currently Amended) A method of simultaneously optimizing performance characteristics in circuit synthesis, comprising the steps of:

(a) generating a set of circuit parameters for each performance characteristic of a circuit;

(b) simultaneously passing each said set of circuit parameters through a respective circuit model, wherein additional sets of circuit parameters may be passed at the same time in parallel;  
[[and]]

(c) running a simulation of each said circuit model on an analysis test bench in order to measure performance of said circuit model using said set of circuit parameters, each said analysis test bench adapted to model circuitry external to said circuit and control the type of analysis to be performed for each said performance characteristic of said circuit; and

(d) receiving the performance measurements for each simulation at an optimizer and determining for which performance characteristics the specifications are met, and, for those analyses where the specifications are not met then generating new parameter values and repeating steps (a) through (d).

2. (Original) A method according to claim 1, further comprising the step of receiving the measurements of performance for each simulation in an optimizer, said optimizer adapted to determine whether specifications were met for said simulation.

3. (Original) A method according to claim 2, further comprising the step of generating new set of circuit parameter values in said optimizer.

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4. (Original) A method according to claim 3, further comprising the step of passing said new set of circuit parameter values through the respective said circuit model.
5. (Original) A method according to claim 1, further comprising the step of assigning each said analysis to a separate processor for parallel processing.
6. (Original) A method according to claim 1, further comprising the step of checking a lookup database for previously optimized performance characteristics.
7. (Original) A method according to claim 1, further comprising the step of saving optimized performance characteristics to a lookup database.
8. (Original) A method according to claim 1, further comprising the step of setting up ranges for each said analysis test bench and providing design parameters using a simulation script.
9. (Original) A method according to claim 1, further comprising the step of mapping the function of a design parameter to a performance characteristic.
10. (Currently Amended) A simulation system for simultaneously optimizing performance characteristics in circuit synthesis, comprising:
  - (a) a set of design parameters for a circuit;
  - (b) at least one circuit model for incorporating said set of design parameters, each said circuit model adapted to model a portion of said circuit pertaining to a performance characteristic, wherein additional sets of circuit parameters may be passed at the same time in parallel; [[and]]
  - (c) at least one analysis test bench connected to each said circuit model, each said analysis test bench adapted to model circuitry external to said circuit and control the type of analysis to be performed for each said performance characteristic of said circuit; and

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(d) an optimizer that determines for which performance characteristics the specifications are met, and, for those analyses where the specifications are not met then generating new parameter values and repeating the simulation with the new parameter values.

11. (Original) A simulation system according to claim 10 additionally comprising an optimizer adapted to collect the results of said analysis of each said analysis test bench and compare said results to optimal performance specifications for said circuit.

12. (Original) A simulation system according to claim 11, wherein said optimizer comprises an optimization algorithm.

13. (Original) A simulation system according to claim 12, wherein said optimization algorithm is adapted to generate parameter values to be passed to each said analysis test bench.

14. (Original) A simulation system according to claim 10, further comprising a simulator for each said analysis test bench.

15. (Original) A simulation system according to claim 10, wherein each said analysis test bench is adapted to run multiple occurrences of said analysis for each said circuit.

16. (Original) A simulation system according to claim 10, wherein said analysis may be performed over multiple operating conditions.

17. (Original) A simulation system according to claim 16, wherein said multiple operating conditions are selected from the group consisting of temperature, supply voltage, and fabrication process.

18. (Original) A simulation system according to claim 10, wherein said circuitry is selected from the group consisting of stimuli, power supplies, and load devices.

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19. (Original) A simulation system according to claim 10, further comprising a processor for each said circuit model.

20. (Original) A simulation system according to claim 10, further comprising at least one simulation script for each said circuit model.

21. (Original) A simulation system according to claim 10, further comprising a synthesis plan adapted to set out rules for said analysis.

22. (Original) A simulation system according to claim 10, further comprising a lookup database.

23. (Original) A simulation system according to claim 22, wherein said lookup database includes a set of performance specifications for each said circuit model.

24. (Original) A simulation system according to claim 10, wherein said design parameters are selected from the group consisting of transistor dimensions, bias current values, and adjustable circuit parameters.